DOCUMENT-IDENTIFIER: US 5926208 A
TITLE: Video compression and decompression arrangement having reconfigurable camera and low-bandwidth transmission capability

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DEPR:
The video communication processor, e.g., a Multimedia Encode Processor ("MEP") available from 8X8, Inc., Santa Clara, Calif., is coupled to main memories SRAM 1033 and DRAM 1027 and second memory 1031. This memory may be ROM, EPROM, EEPROM, flash EPROM or some other type of memory. One obstacle to downloading an entire compression module from the computer system 1002 to the MEP 1024 is the large magnitude of the compression module, requiring a large physical size of on-board memory. For example, the cells of a standard RAM **chip** are almost four times larger than the cells of a standard ROM. Therefore, to maintain the small physical size of the on-board memory but still allow a variety of different compression modules to be downloaded, two types of memory are used:

the larger RAM type and the smaller ROM type. The larger memory is exemplified in FIG. 2 as, for example, an SRAM 1033 or DRAM 1027, and the smaller memory is exemplified in FIG. 2 as, for example, a ROM 1031. The first ROM memory stores subroutines, or subprograms, that are executed on an as-needed basis in connection with the execution of any one of the compression modules, which is downloaded into the RAM type memory. Because a ROM cell is about one-fourth the physical size of a RAM cell, the storage of these subprograms on ROM results in a significant savings in memory, and enables the video camera 1000 to execute one of a variety of compression programs downloaded to the camera without the burdens to camera size, extra equipment, real estate and cost associated with increased memory space.

DEPR:
Referring now to FIG. 3, there is shown a detailed disclosure of the video communication processor 1024 known as the MEP comprising a video processor (VP) 1036, RISC processor 1038 and video source inputs 1040 from a video source 1030. The MEP 1024 is a single-**chip** programmable video codec and multimedia communications processor suitable for a variety of applications. The MEP requires only memory and interface circuits for implementation of a complete multimedia and conferencing subsystem. In

one video conferencing application, the MEP acts as a full CIF (common interchange format) resolution, H.261 codec with forward error correction and audio/video bit stream multiplexing and demultiplexing according to the H.320 which includes the H.221, H.230, H.242, H.243, and H.261 digital communication standards described in recommendations from the CCITT (International Telegraph and Telephone Consultation Committee).

DEPR:
The SRAM interface 202 controls accesses to mapped I/O devised such as standard SRAM or non-volatile memory (ROM, EPROM, EEPROM, and flash). A data 32-bit data bus LD[31:0] and a 20-bit address bus LA[19:0] connects the SRAM interface 202 with the external SRAM 152, but the memory interface 202 also supports 16-bit and 8-bit devices. Signals on four byte enable lines, LWRLL, LWRLH, LWRHL, and LWRHH, determine which bytes in a 32-bit word are written to the external SRAM 152. The SRAM interface 202 supports four independent external address spaces for four banks of memory or mapped I/O devices. Four **chip** enable lines LCE[3:0] from the SRAM interface 202 select the address space being accessed. Each address space has programmable bus width and wait-states. The SRAM interface 202 and the RISC processor 1038 thus supports varied types of memories including SRAM, ROM, EPROM,

EEPROM, and flash and memory mapped I/O devices.

DEPR:
Referring now to FIG. 8a, there is shown an embodiment of the video source 1030. The video source 1030 comprises a charge-coupled device (CCD) 2034 for capturing images, an analog signal processor (ASP) 2038, an analog-to-digital converter (ADC) 2040, and a digital processing **chip** (DPC) 2042. The CCD 2034 has a plurality of control inputs 2036 coupled to a control output 2056 of the DPC 2042 for receiving camera configuration information from the MEP 1024. The CCD 2034 has a plurality of video outputs 2044 coupled to an input 2046 of the ASP 2038 to allow an analog image signal captured by the CCD 2034 to be formatted for subsequent conversion into digital form. The ASP 2038 has an output 2048 coupled to an input 2050 of ADC 2040 to allow the formatted analog signal to be converted to a digital signal before transmission to the MEP 1024 for compression. The ADC 2040 has an output 2052 coupled to a video input 2058 of the DPC 2042 to allow transmission of the digital signal to reach the MEP 1024. The DPC 2042 has a video output 2060 coupled to the MEP 1024 to send the digital video signal to the MEP 1024 to be compressed. In an embodiment of the present invention, video source 1030 is an Eyecam.TM. model digital camera

manufactured by Silicon Vision of Fremont, Calif.

DEPR:
The external SRAM 152 acts as FIFO storage for the numerous buffering operations and eliminates on-**chip** FIFOs. In some applications, external FIFO buffers between VCP and external devices are not needed because the RISC processor 1038 is programmed to create FIFO buffers in the SRAM 152. In many systems, the TDM interface 215 connects to an ISDN shipset and the audio port 213 connects to audio DACs or to a DSP for audio processing. Software executed by the RISC processor 1038 can reserve memory space in the SRAM 152 for data transfers to or from TDM and the audio interfaces 213 and 215 so that additional external buffers are not required.